Performance Analysis of Gigabit Ethernet Shared-Memory Switch with Embedded-DRAM

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Outline

- Motivation
- Background
- Previous Works
- Modeling of Shared-Memory Switch
- Performance Analysis with General Policy
- Performance Analysis with Dedicated Policy
- Conclusion

Motivation

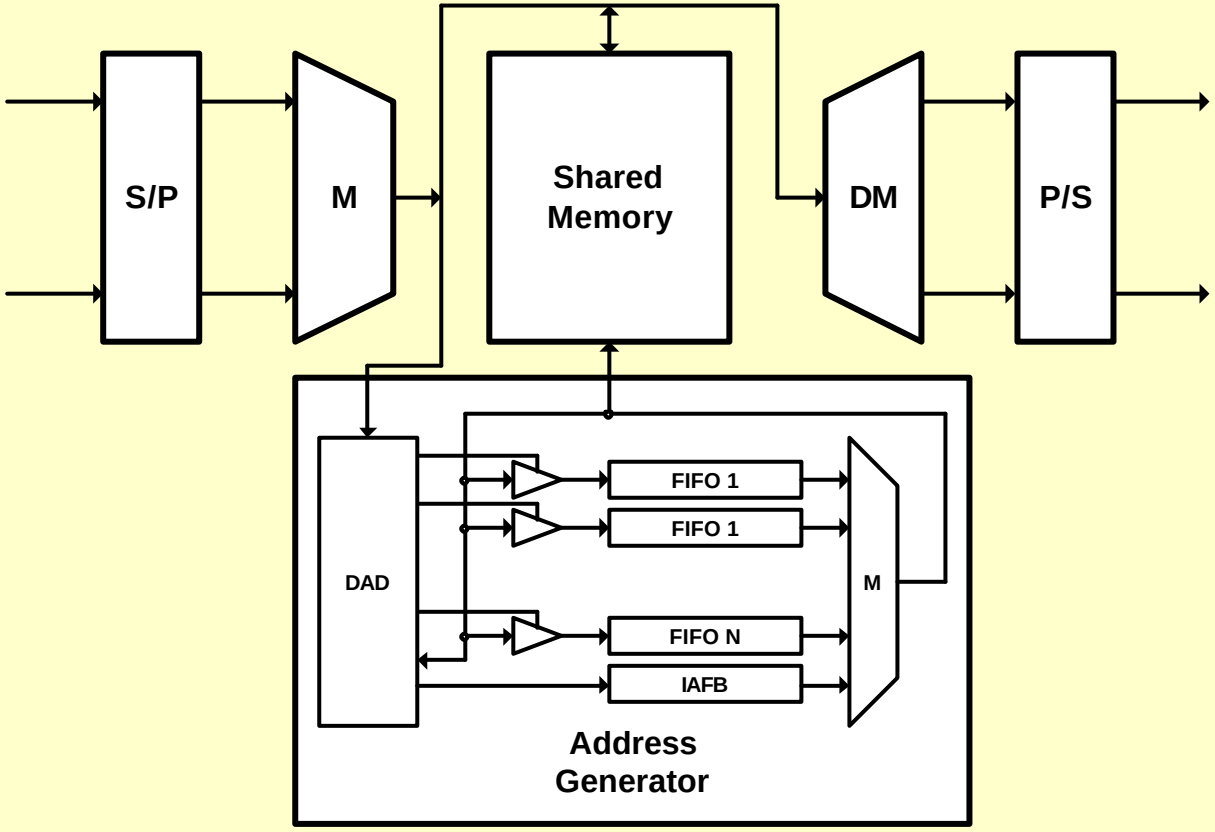
- Multimedia data (data/voice/video) is increasing network traffic.
- Network switch is required to have large buffer due to large packet size (1.5kbyte) and bursty traffic pattern.
- DRAM is being used as packet buffers.

Background

- Function of Switch
  - Routing
  - Buffering (Output conflict)
- Ideal Switch
  - Non-blocking
  - Work-conserving
- Performance Index of Switches
  - Throughput
  - Average Waiting Time
  - Packet Loss Probability

Background

- Shared-Memory Switch Architecture



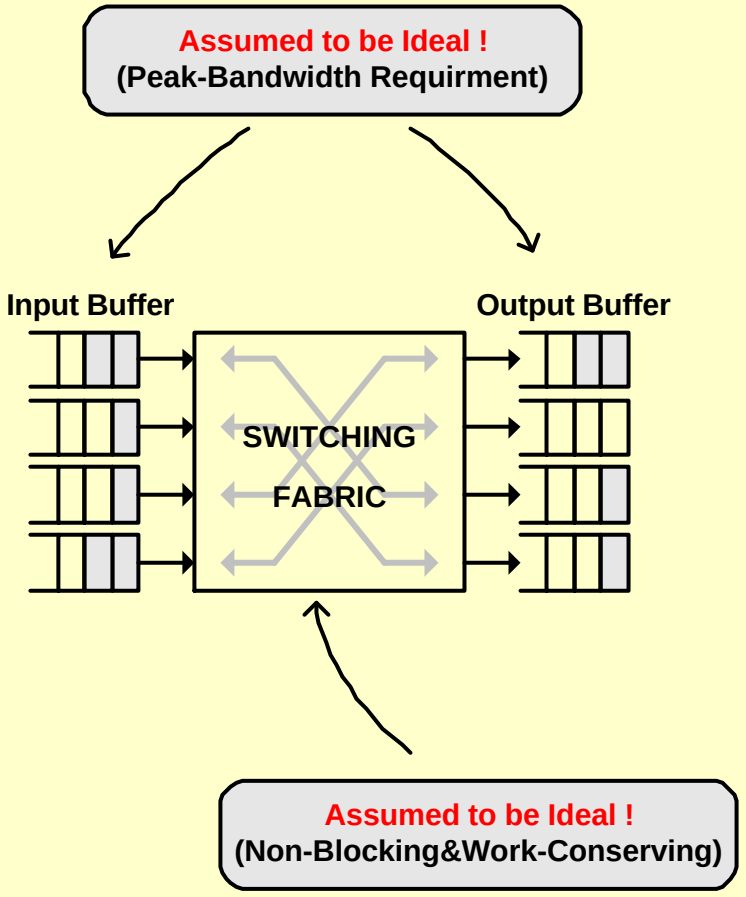
Hybrid Shared and Dedicated Output Buffer Switch

Background

- Input Traffic Patterns
  - Independent uniform traffic pattern (Bernouilli process)
    - The requested output port for a packet is uniformly chosen among all output ports, independently for all arriving packets.
  - Bursty traffic pattern
    - Packets in a burst destined to the same output port.

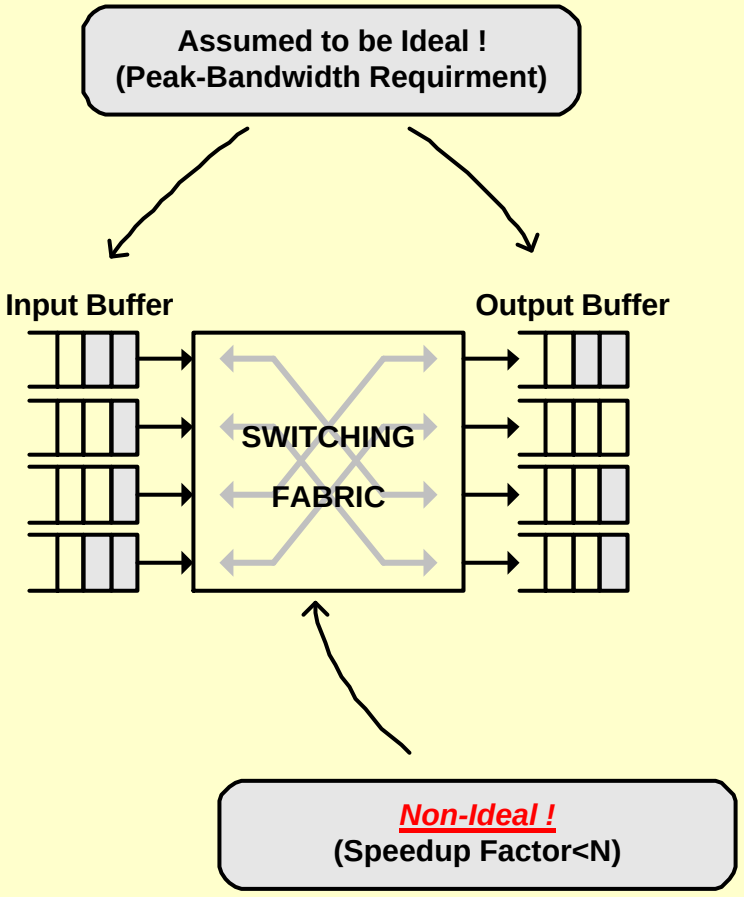
Previous Works

- Queueing Theory
  - Mark J. Karol, “Input vs. output queueing on a space-division packet switch,” 1987.
  - Michael G. Hluchyj, “Queueing in high-performance packet switching” 1988.



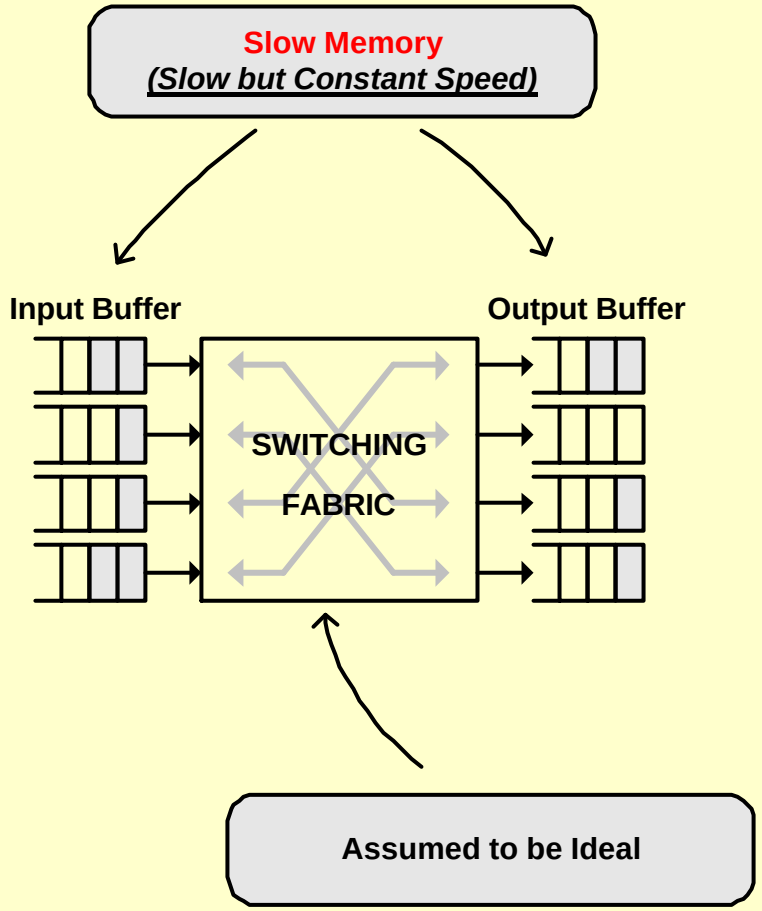
Previous Works

- Non-Ideal Switching Fabric
  - Achille Pattavina, “Analysis of input and output queueing for non-blocking ATM switches,” 1993.
  - I.I. Makhamreh, “ Analysis of an output buffered ATM switch with speed-up constraints,” 1995.



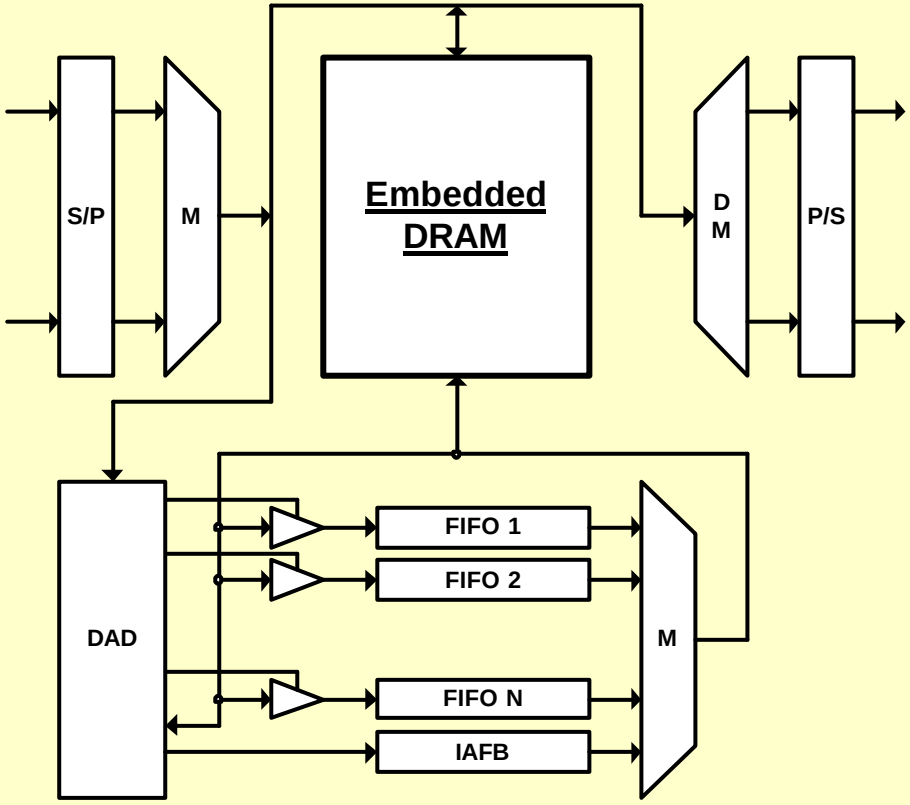
Previous Works

- Slow Buffer
  - Sundar Iyer, “Analysis of a packet switch with memories running slower than the line-rate,” 2000.



Modeling of Shared-Memory Switch

- Reference Architecture



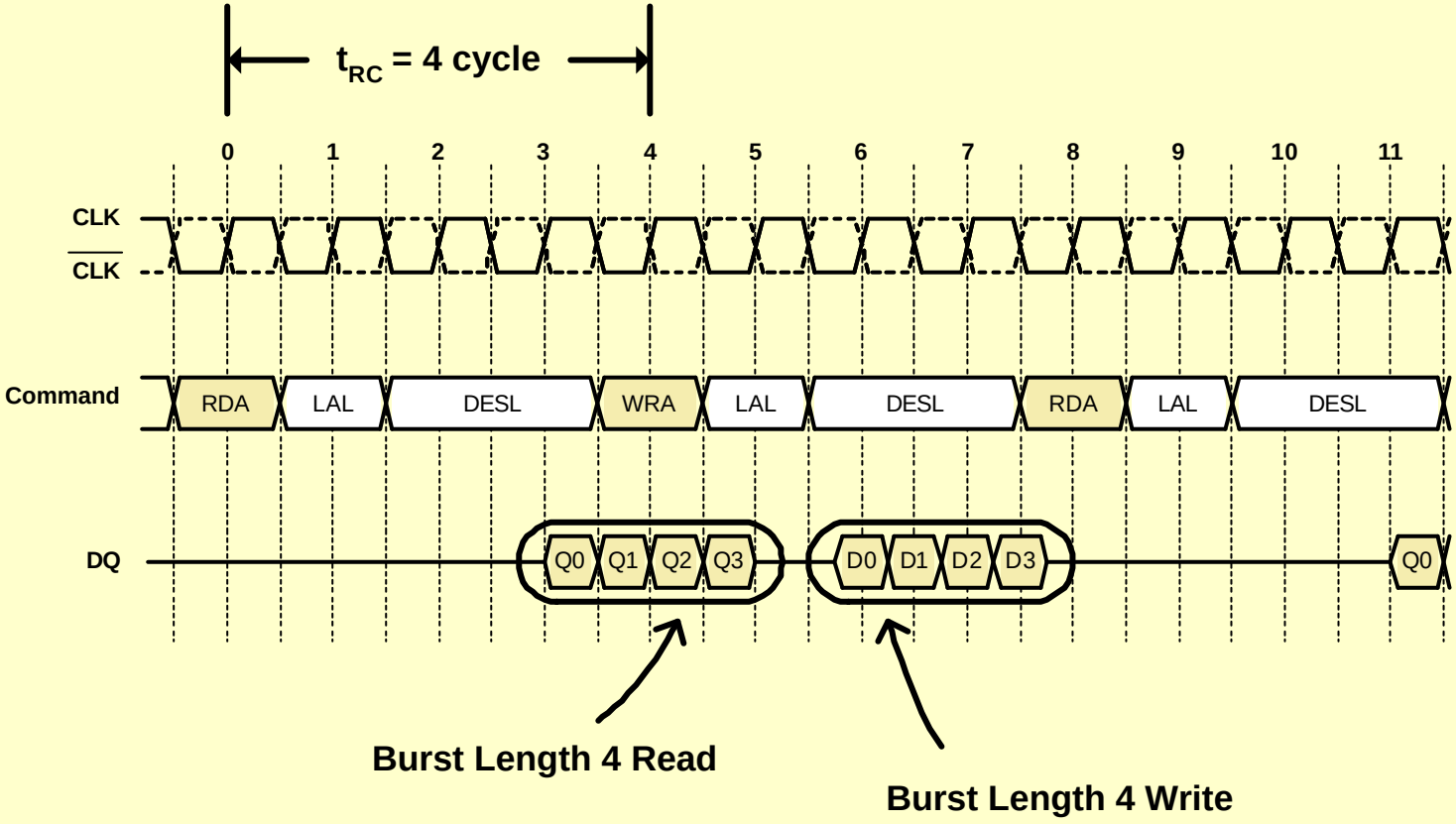
Hybrid Shared and Dedicated Output Buffer Switch

Modeling of Shared-Memory Switch (Cont'd)

- Feature Selection

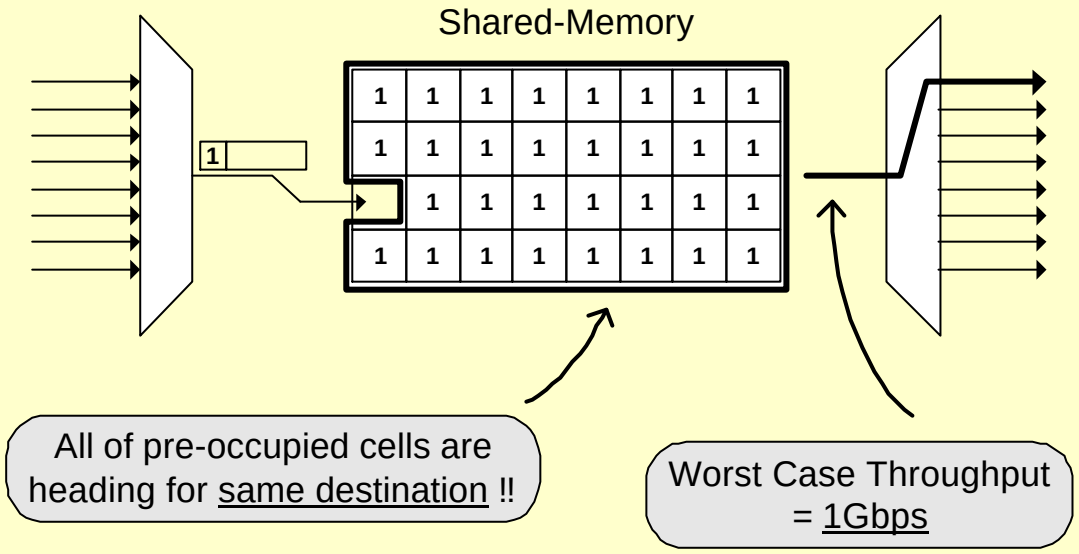
Packet Offering	Line-Rate	1Gbps
	No. of Port	8
	Packet Size	46byte ~ 1500byte
Memory	Clock	125MHz
	I/O bitwidth	128bit
	Capacity	2Mbit
	t_{RC}	32ns(4cycle)
	Burst Length	4

Modeling of Shared-Memory Switch (Cont'd)



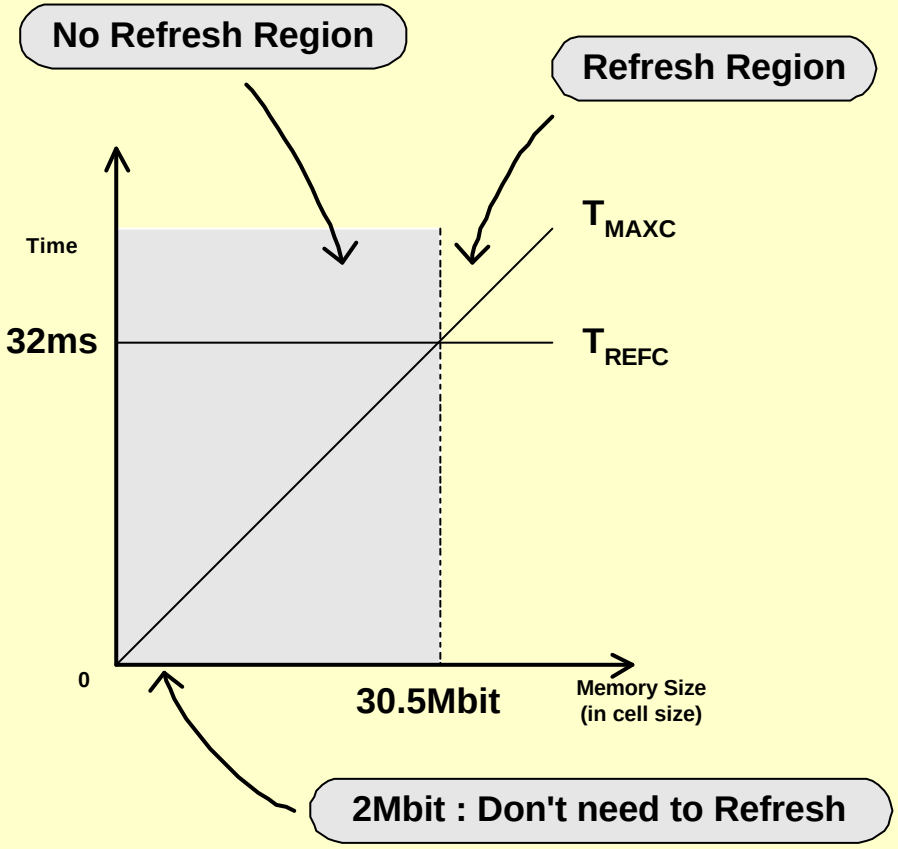
Modeling of Shared-Memory Switch (Cont'd)

- Refresh Consideration



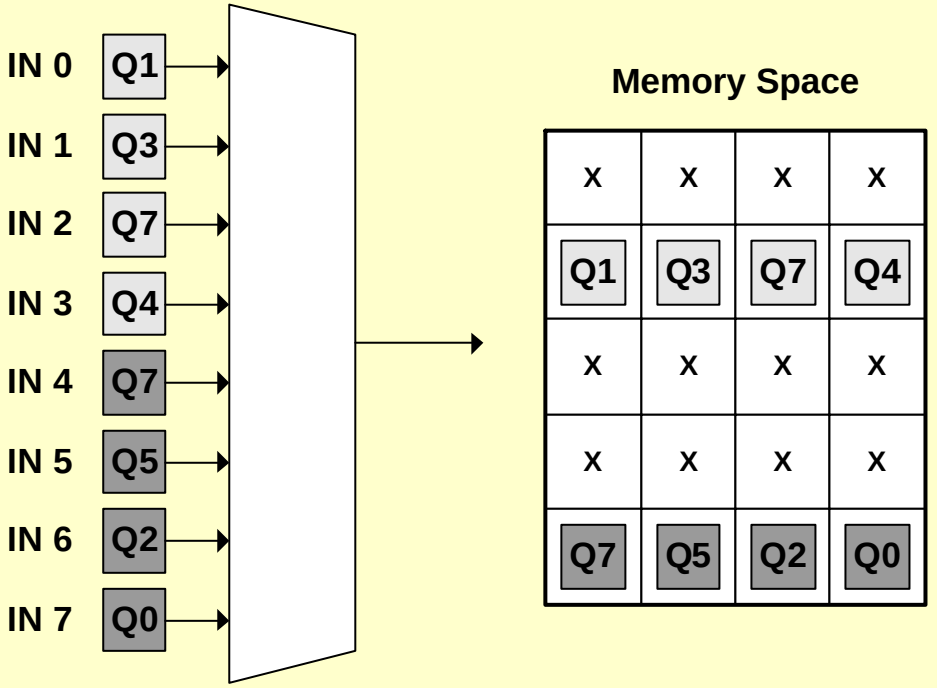
$$T_{MAXC} = \frac{\text{Memory Capacity (bit)}}{\text{1Gbps}} \leqq 32\text{ms}$$

Modeling of Shared-Memory Switch (Cont'd)



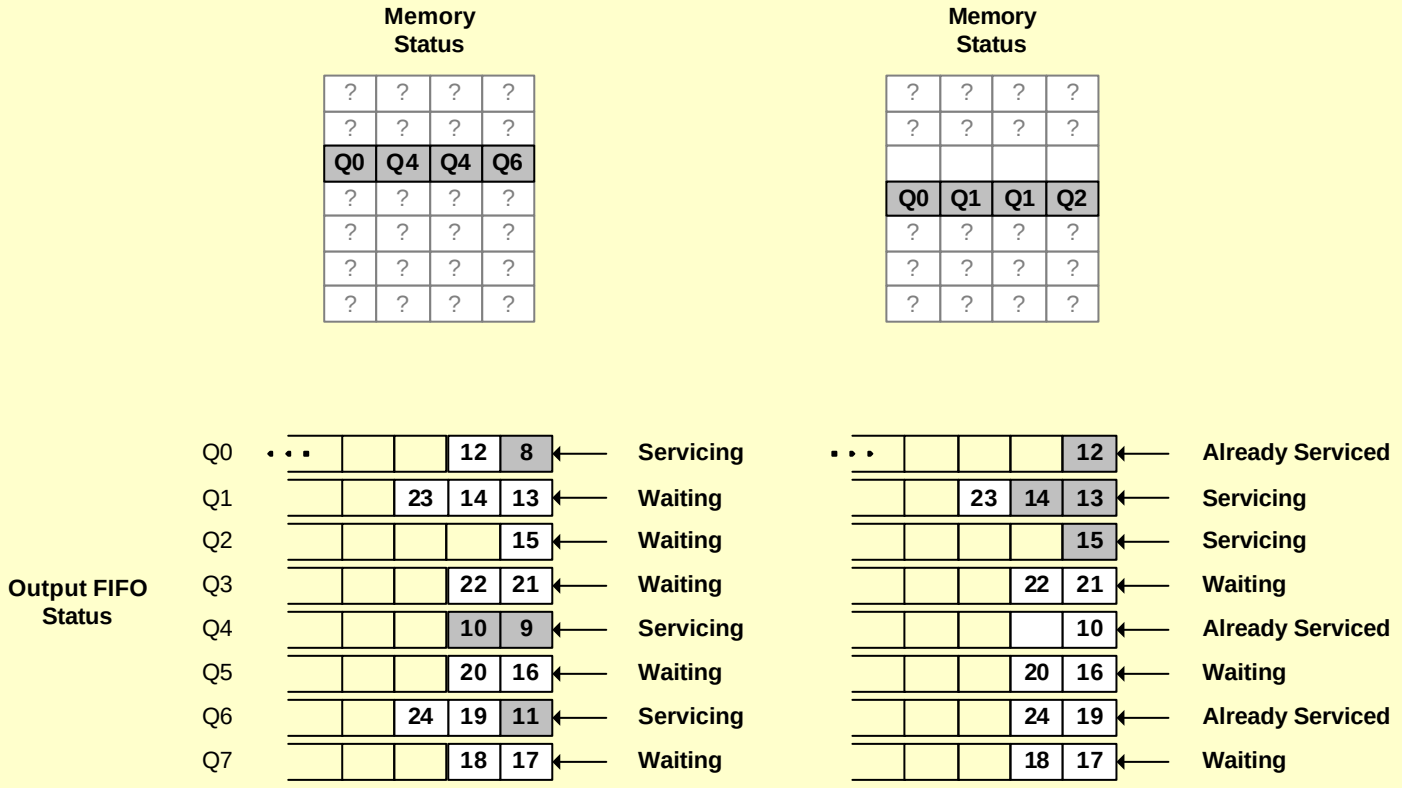
Modeling of Shared-Memory Switch (Cont'd)

- Write Operation of Embedded DRAM Switch



Modeling of Shared-Memory Switch (Cont'd)

- Read Operation of Embedded DRAM Switch

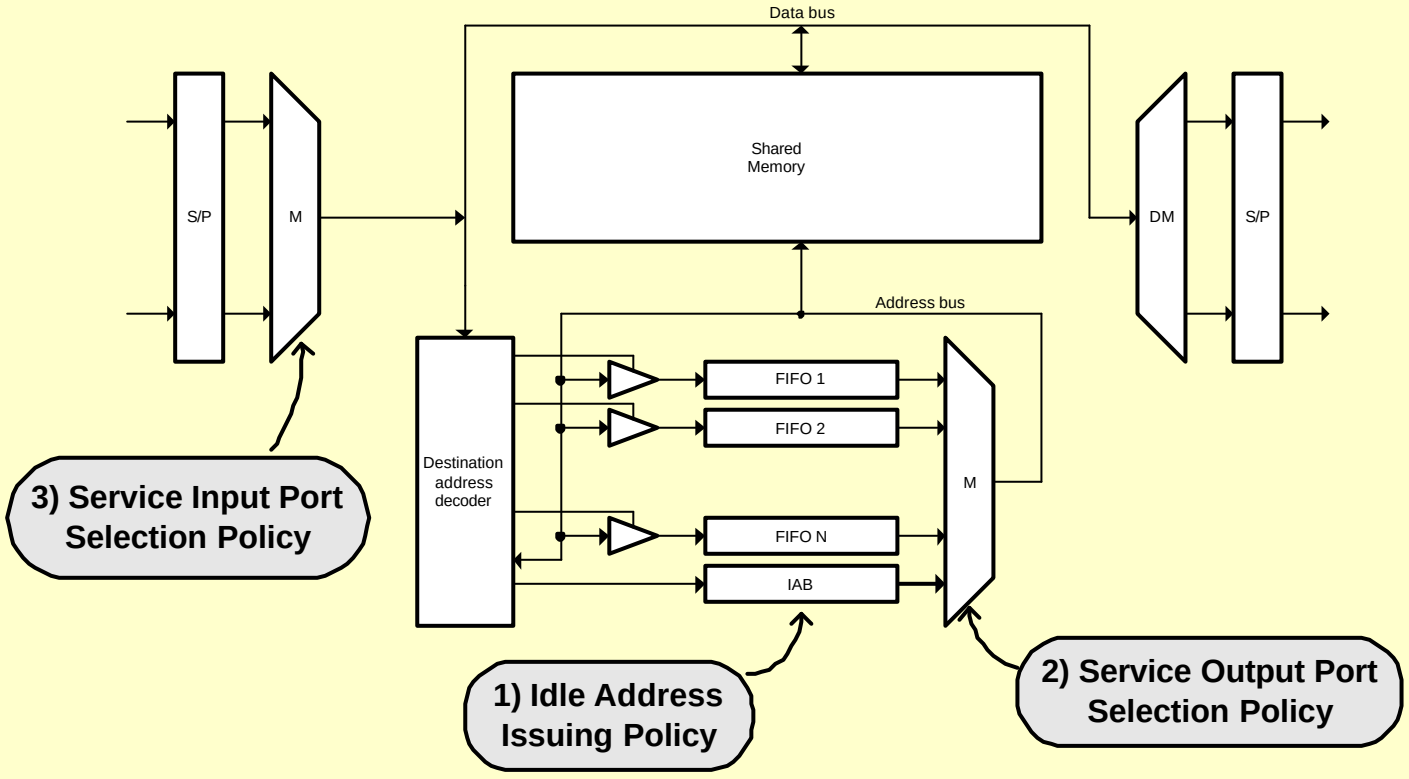


P.A. with General Policy

- Simulation Environment
  - Packet Arrival Process
    - Bernoulli process with parameter p (offered load)
  - Packet Size Distribution
    - Poisson distribution
    - Mean packet size = 616byte
      (from “IEEE workstation mix” distribution, 1996)
  - Packet Chopping
    - Divided into 1~94 cells

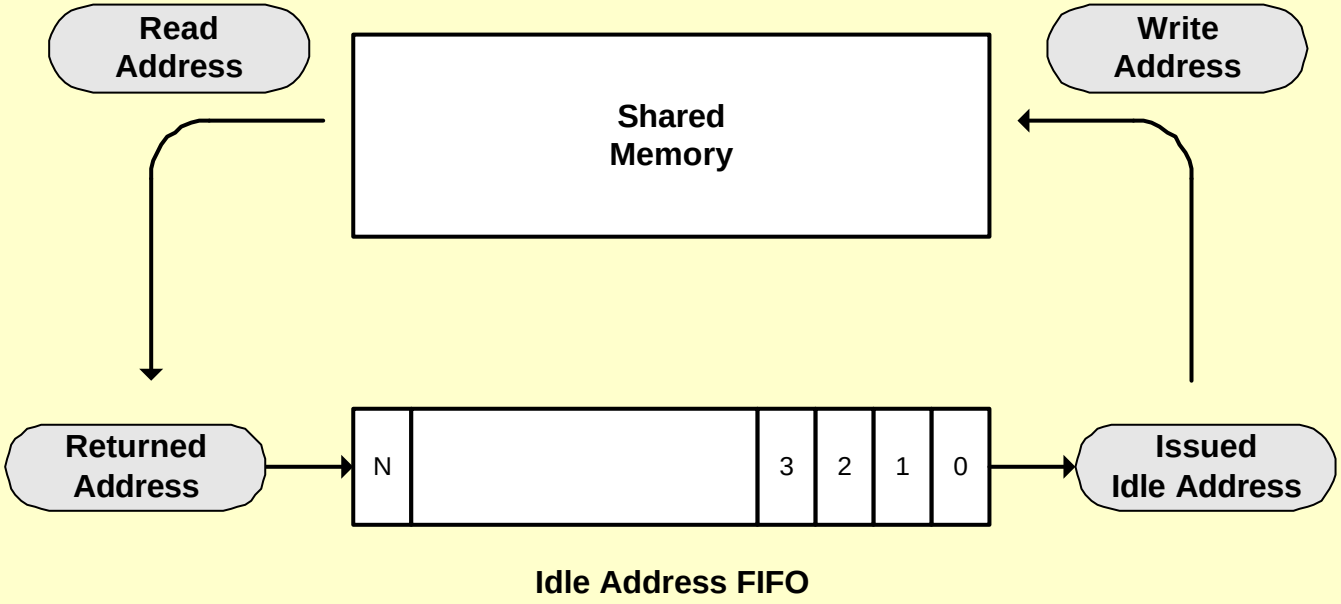
P.A. with General Policy (Cont'd)

- Factors Affecting Memory Access Pattern



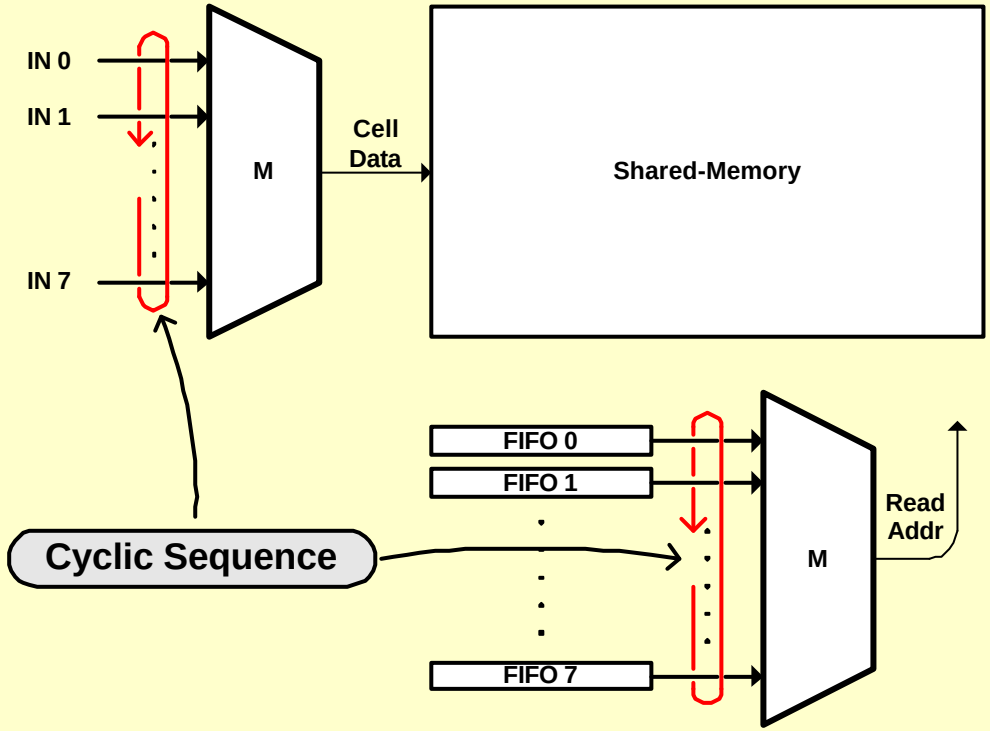
P.A. with General Policy (Cont'd)

- Idle Address Issuing Policy



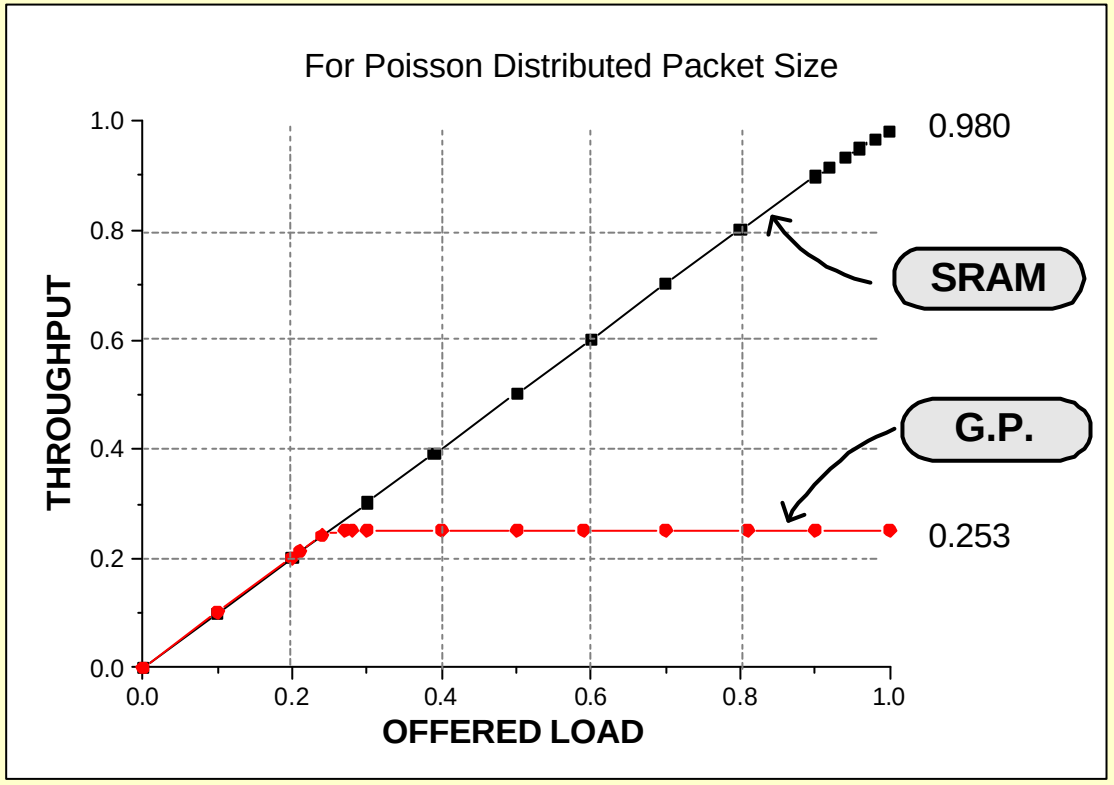
P.A. with General Policy (Cont'd)

- Service Port Selection Policy



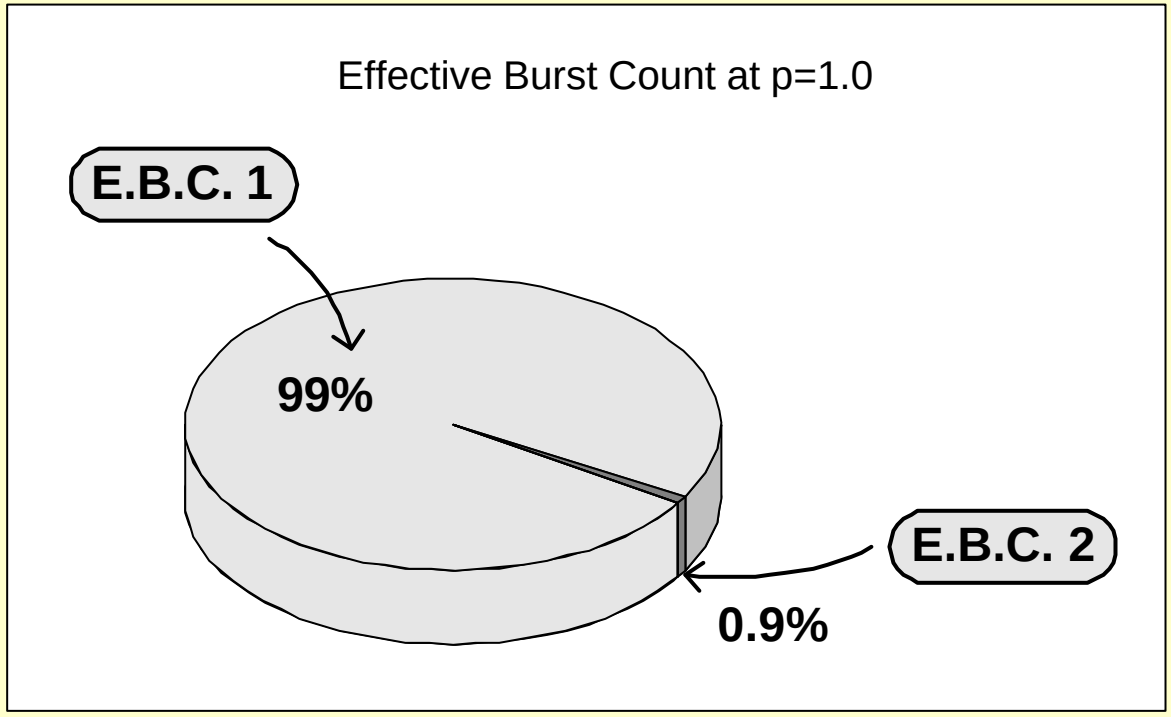
P.A. with General Policy (Cont'd)

- Offered Load versus Throughput



P.A. with General Policy (Cont'd)

- Effective Burst Count for Burst Read



P.A. with General Policy (Cont'd)

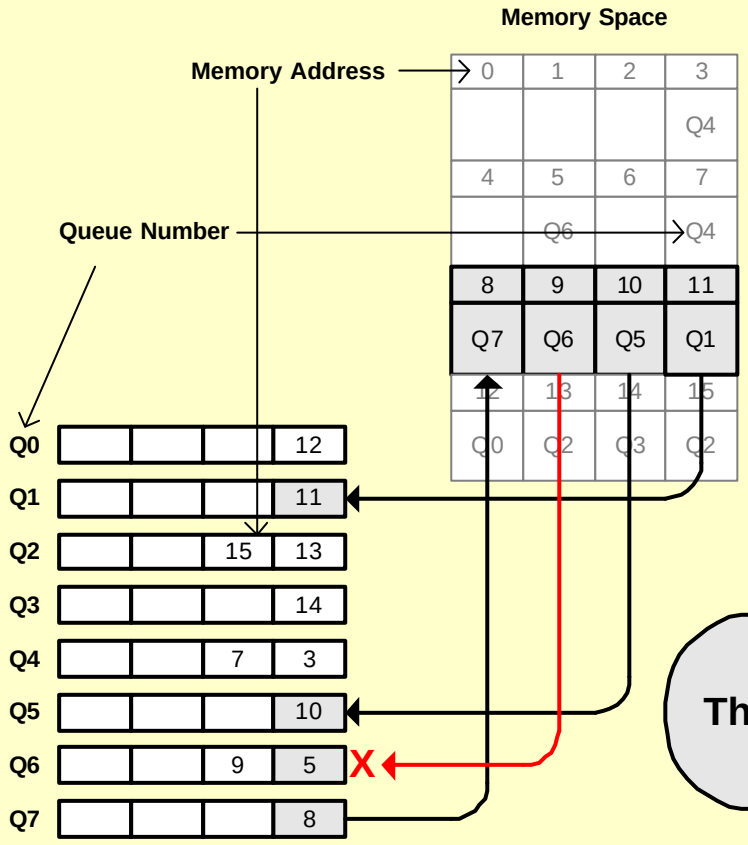
- Conclusion about General Policy
  - FIFO is inadequate for Idle Address Buffer
    - Address reordering is required.
  - Dedicated service output port selection policy is required.
    - Effective Burst Read count must be increased.

→ Dedicated Address Issuing Policy is required!

P.A. with Dedicated Address Issuing

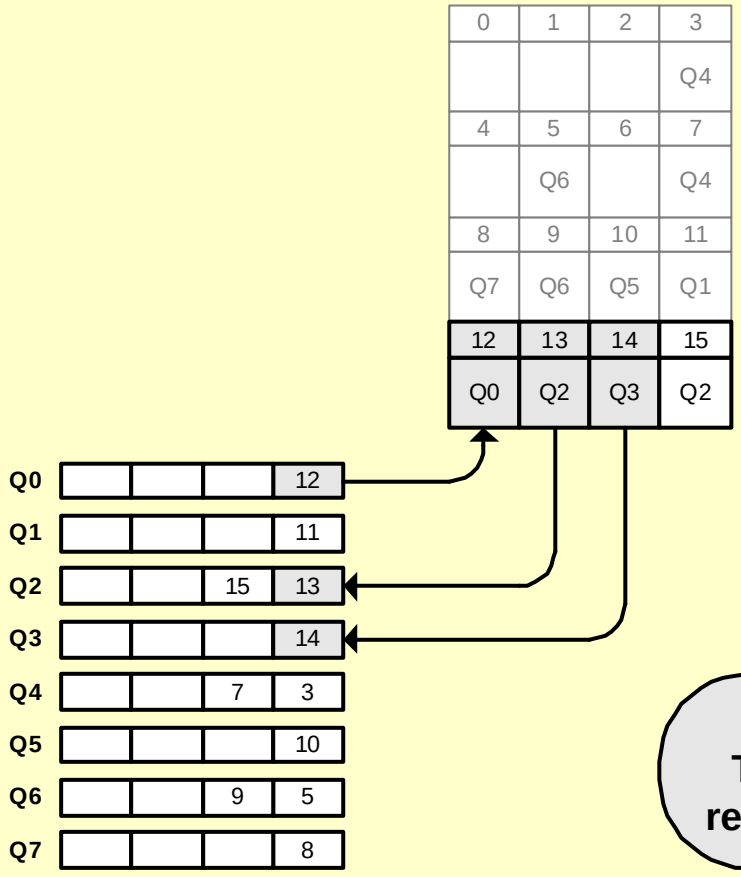
- Dedicated Read Address Issuing
  - Burst read-conserving : A read operation is burst read-conserving if all of the output ports that corresponds to the destination of the retrieved data are serviced.
  - If a read operation is burst read-conserving, the read operation is the best choice to obtain maximum output port utilization, i.e. maximum throughput.

P.A. with Dedicated Address Issuing (Cont'd)



non burst read-conserving !
There is a Q6 data in burst read, but it can not be transmitted .

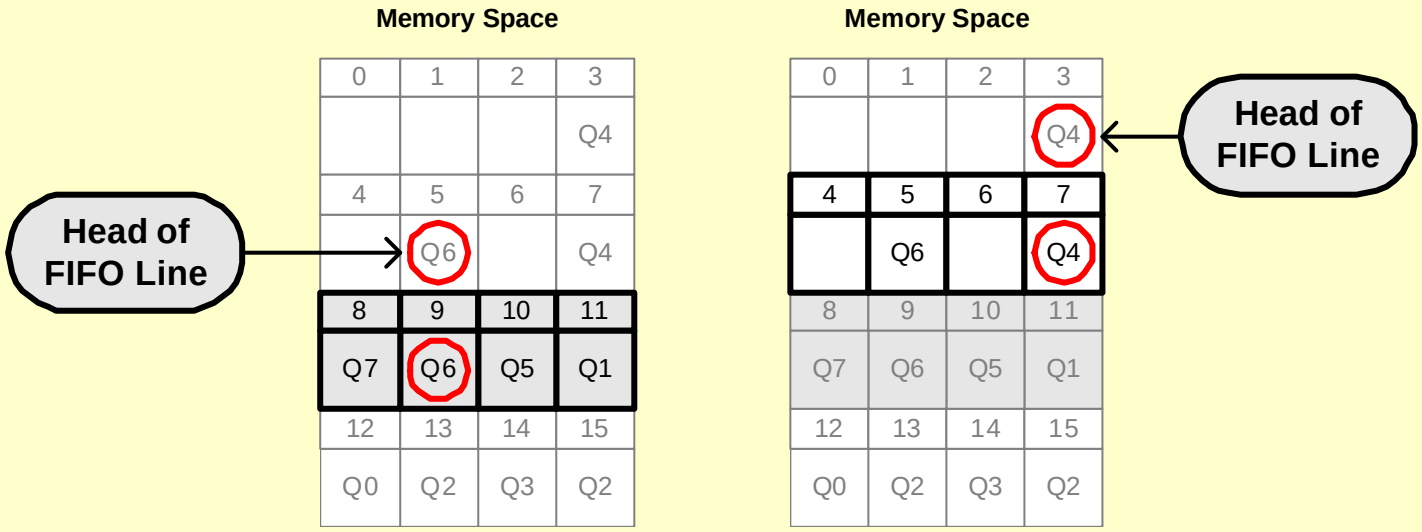
P.A. with Dedicated Address Issuing (Cont'd)



burst read-conserving !
There are Q0, Q2, Q3 data in burst read, and Q0, Q2, Q3 are all serviced.

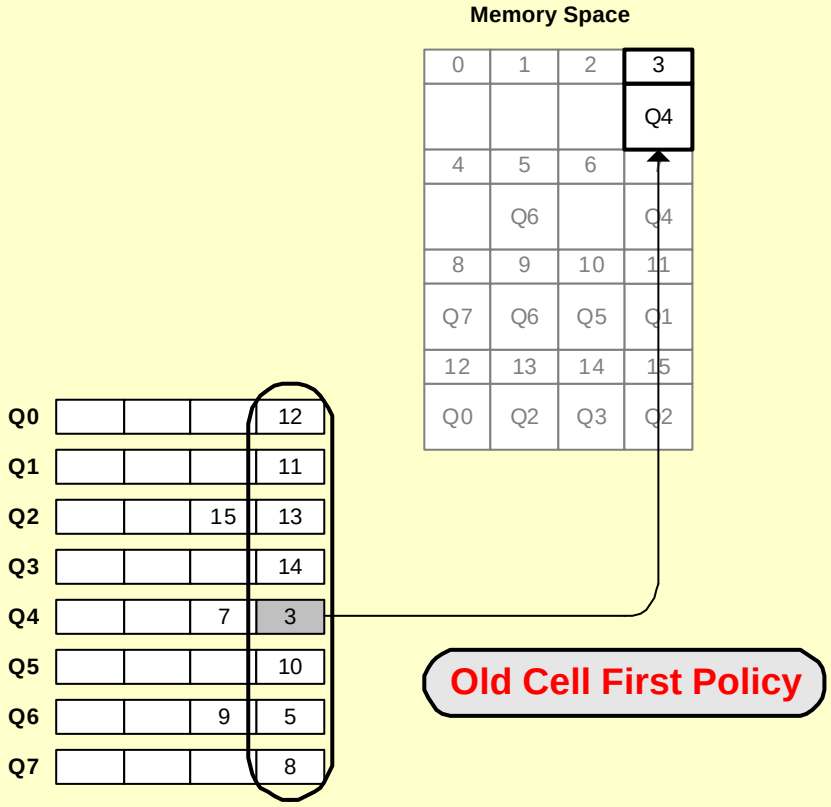
P.A. with Dedicated Address Issuing (Cont'd)

- Burst read-conserving condition



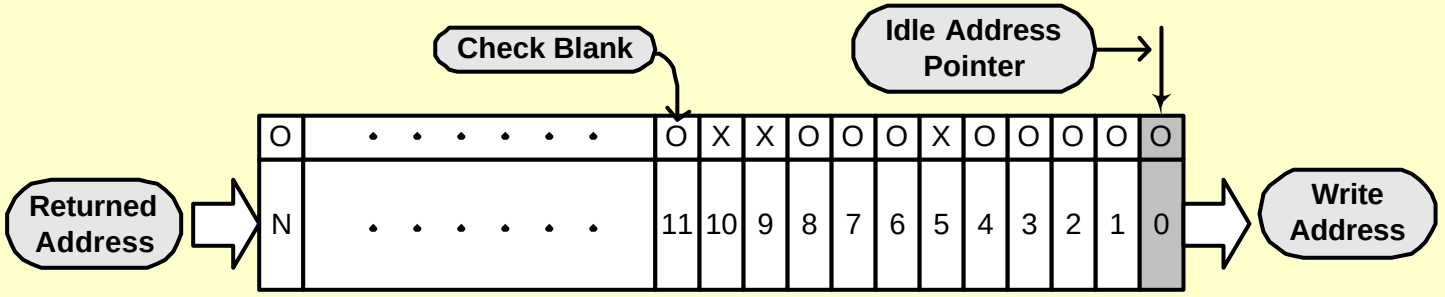
P.A. with Dedicated Address Issuing (Cont'd)

Dedicated Output Port Selection



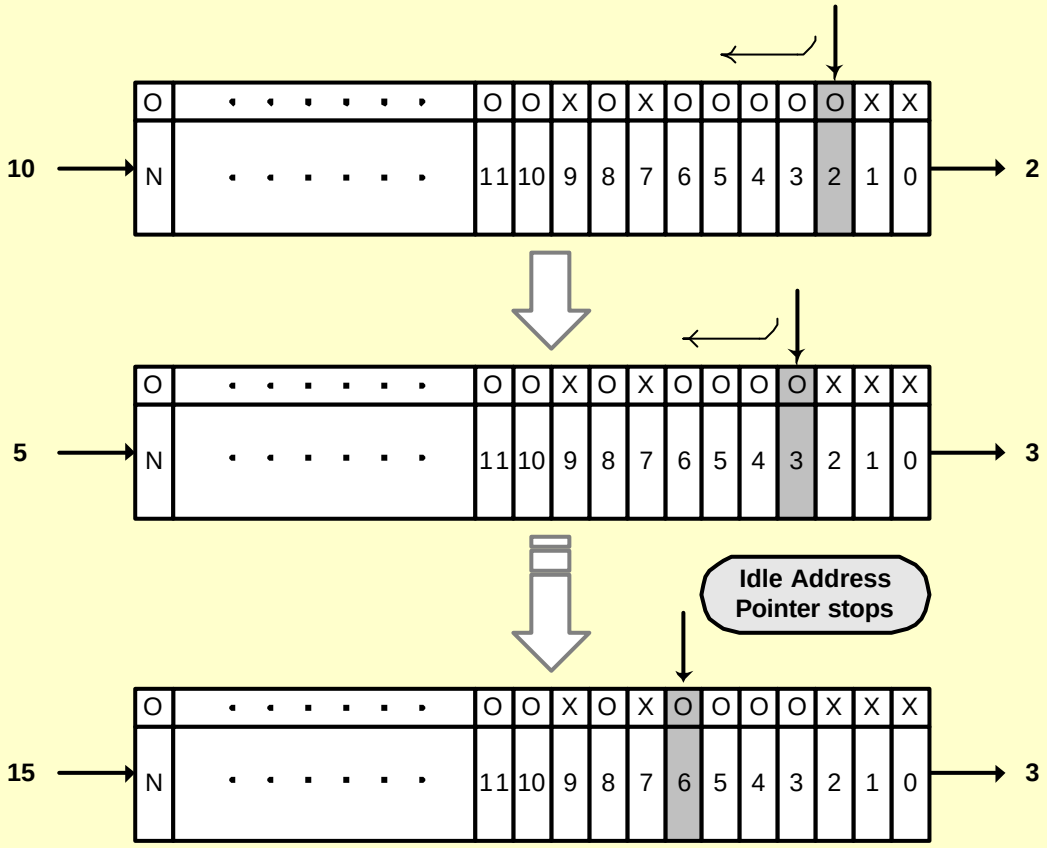
P.A. with Dedicated Address Issuing (Cont'd)

- Dedicated Write Address Issuing
  - Idle Address List



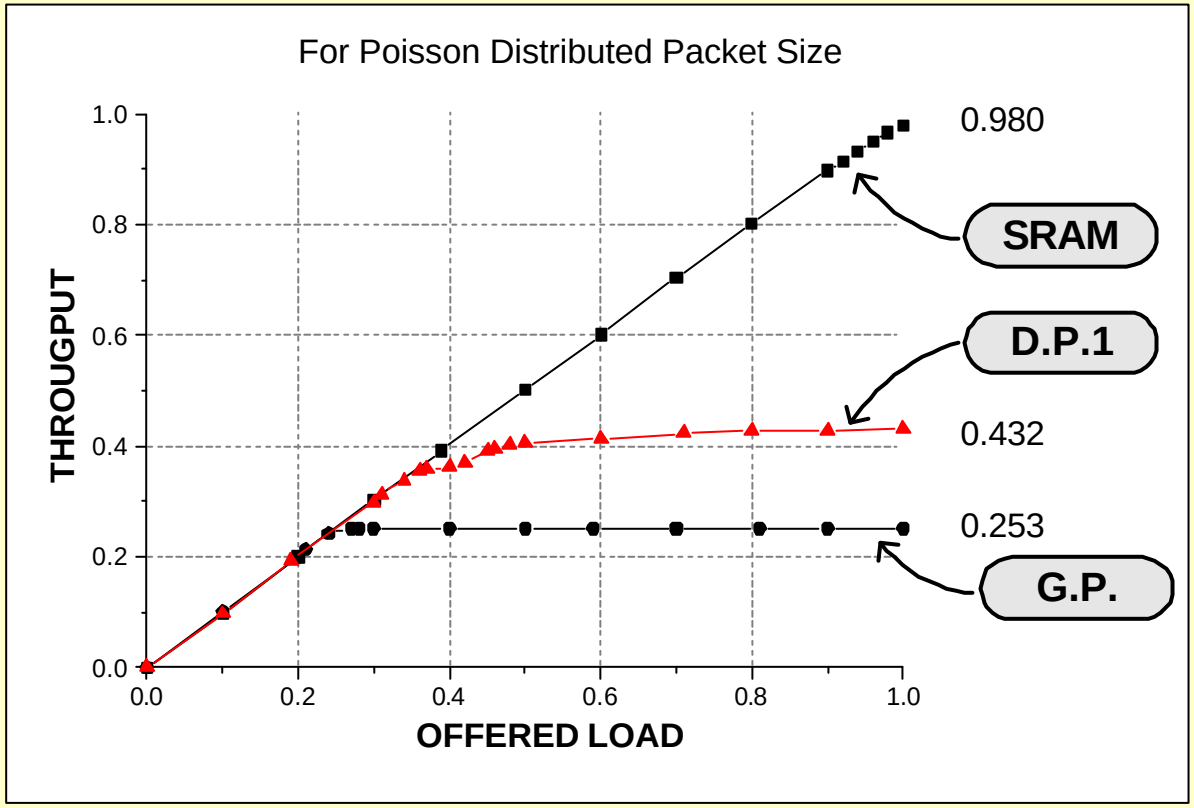
Idle Address List

P.A. with Dedicated Address Issuing (Cont'd)



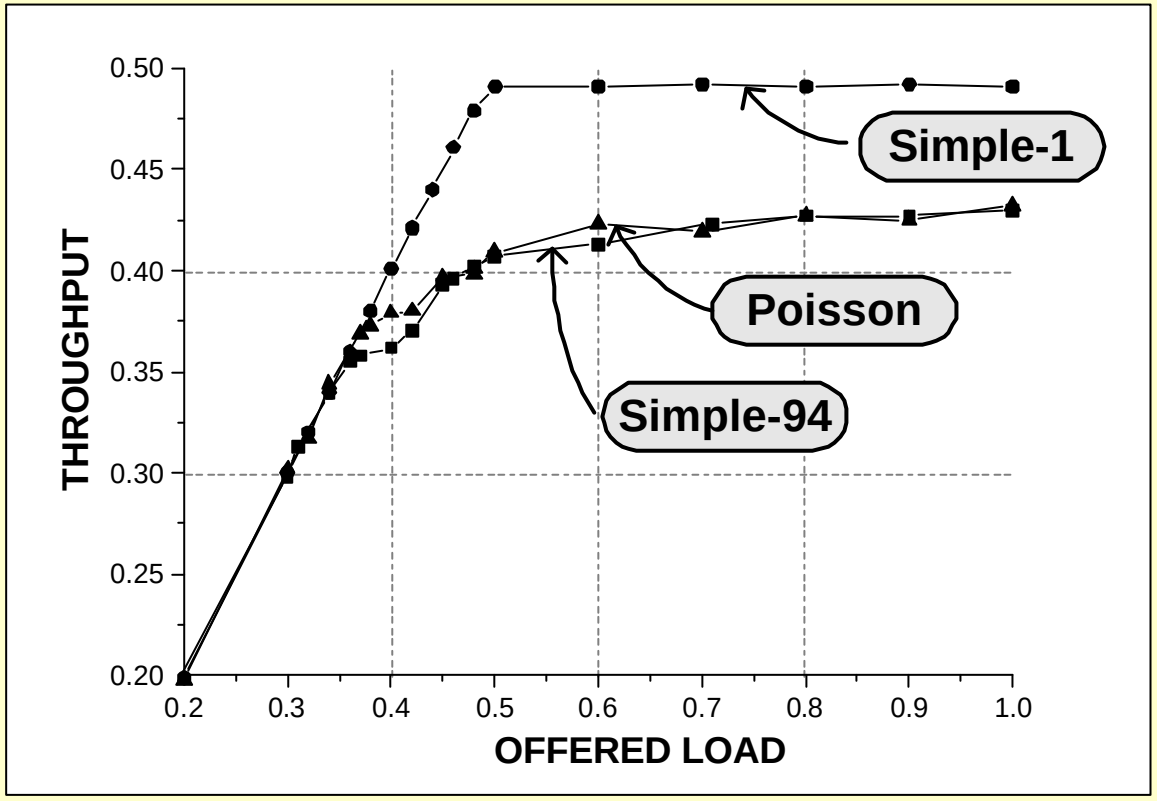
P.A. with Dedicated Address Issuing (Cont'd)

- Throughput versus Offered Load



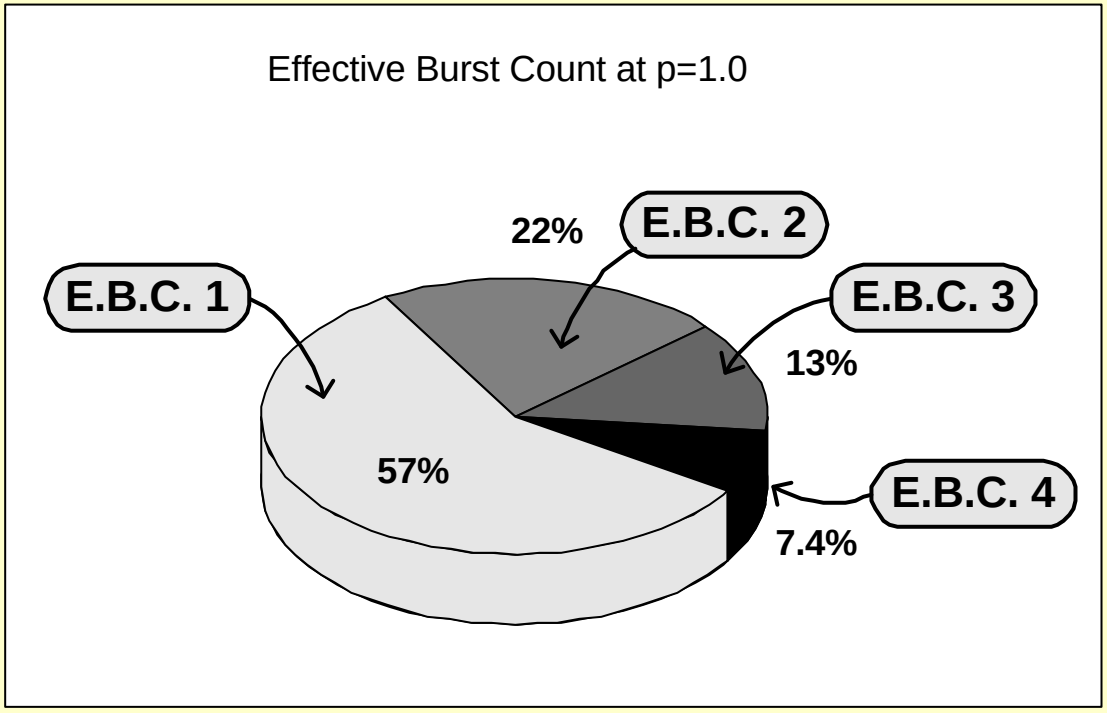
P.A. with Dedicated Address Issuing (Cont'd)

- Throughput Sensitivity for Input Pattern



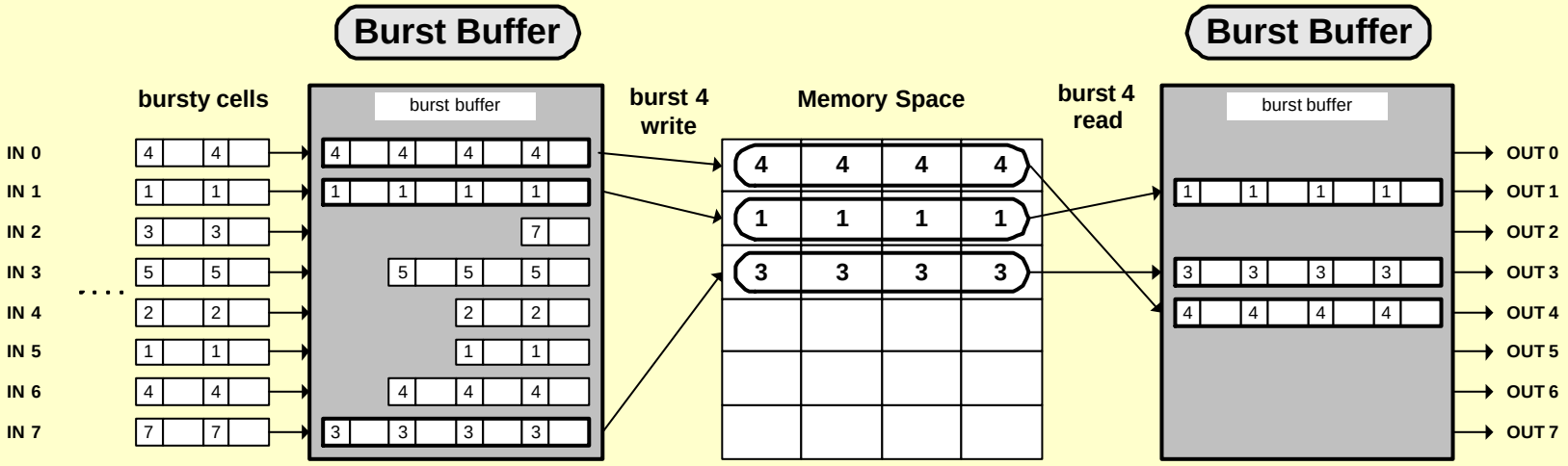
P.A. with Dedicated Address Issuing (Cont'd)

- Effective Burst Count



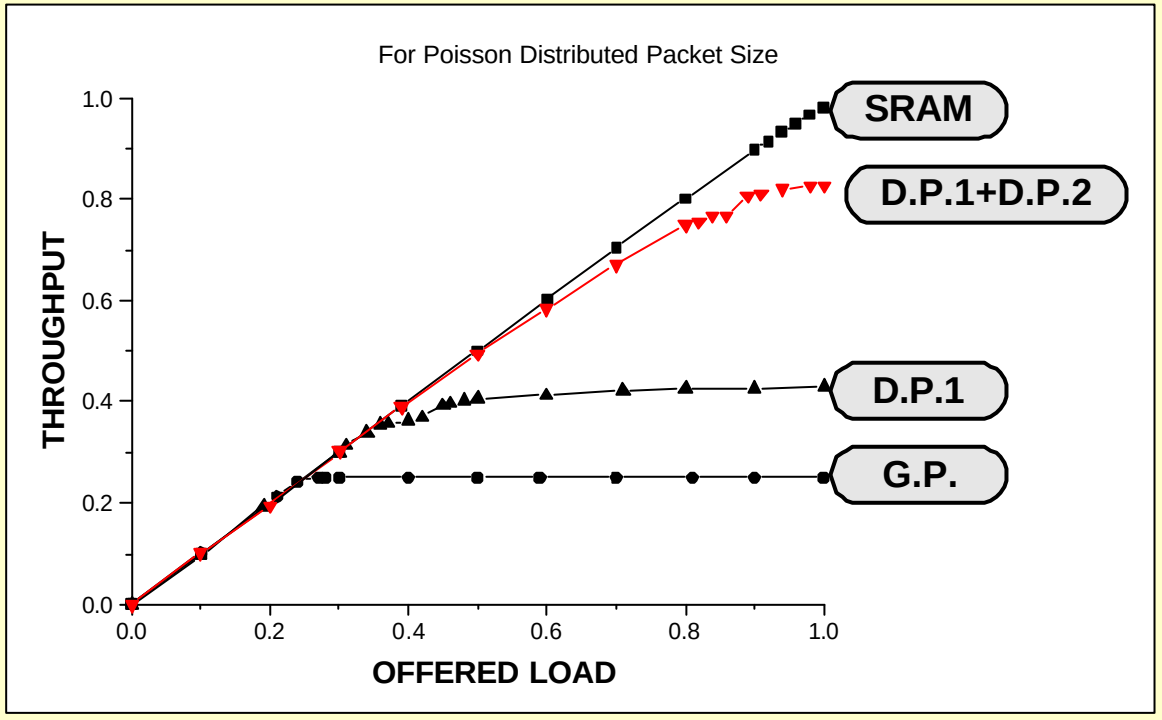
P.A. with Dedicated Service Port Selection

- Burst Port Selection Policy



P.A. with Dedicated Service Port Selection (Cont'd)

- Throughput versus Offered Load

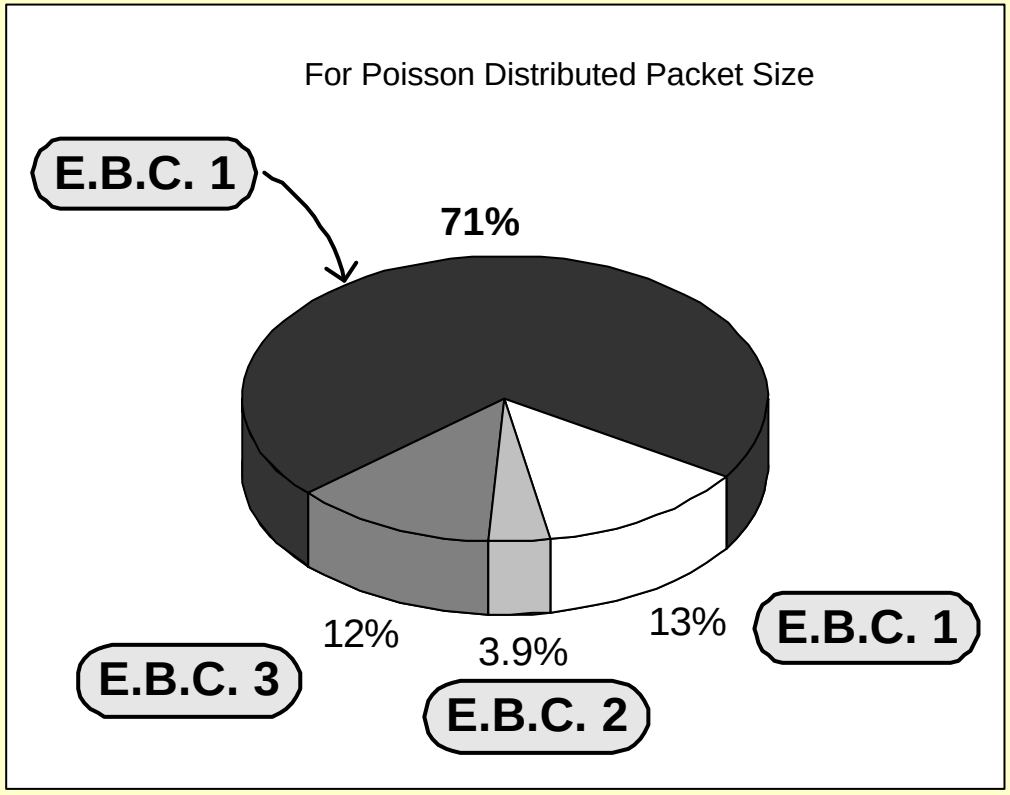


P.A. with Dedicated Service Port Selection (Cont'd)

- Throughput Sensitivity for Input Pattern

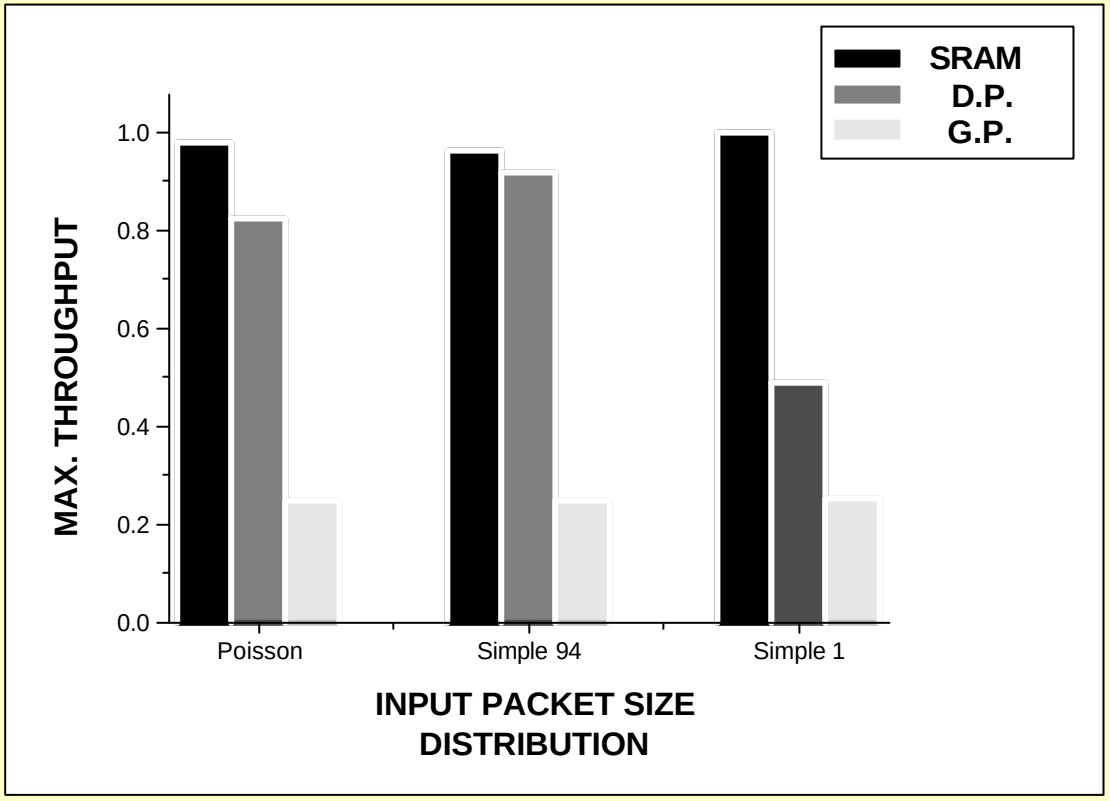
P.A. with Dedicated Service Port Selection (Cont'd)

- Effective Burst Count



Conclusion

- Summary of Performance Analysis



Conclusion (Cont'd)

- With the dedicated address issuing/service port selection policies, the throughput of the embedded-DRAM shared-memory switch showed 15% degradation compared with that of SRAM switch.

- In the condition of large packet size (1500byte), the throughput degradation was 5%.

- If the switch is applied to the bursty traffic networks like Gigabit Ethernet, the performance degradation will be negligible.